

ESD-TR-66-396

# ESD RECORD COPY

RETURN TO  
SCIENTIFIC & TECHNICAL INFORMATION DIVISION  
(ESTI), BUILDING 1211

ESD ACCESSION LIST

ESTI Call No. AL 52041

Copy No. 1 of 1 copy

Technical Note

1966-39

J. D. McCarron

Diamond Circuit  
Considerations

21 July 1966

Prepared under Electronic Systems Division Contract AF 19(628)-5167 by

**Lincoln Laboratory**

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Lexington, Massachusetts



ESRL

AD0637166

The work reported in this document was performed at Lincoln Laboratory,  
a center for research operated by Massachusetts Institute of Technology,  
with the support of the U.S. Air Force under Contract AF 19(628)-5167.

This report may be reproduced to satisfy needs of U.S. Government agencies.

Distribution of this document is unlimited.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
LINCOLN LABORATORY

DIAMOND CIRCUIT CONSIDERATIONS

*J. D. McCARRON*

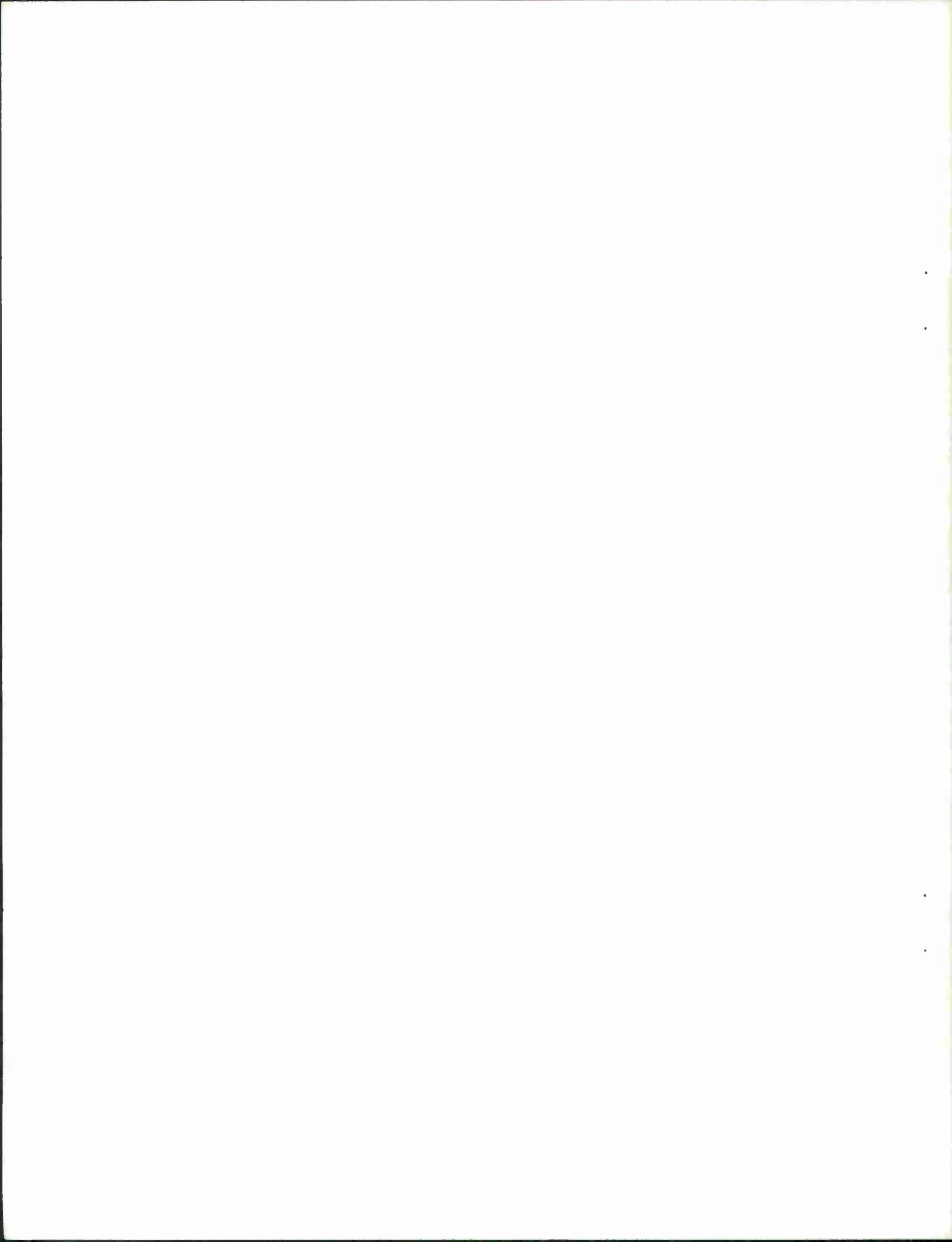
*Group 63*

TECHNICAL NOTE 1966-39

21 JULY 1966

LEXINGTON

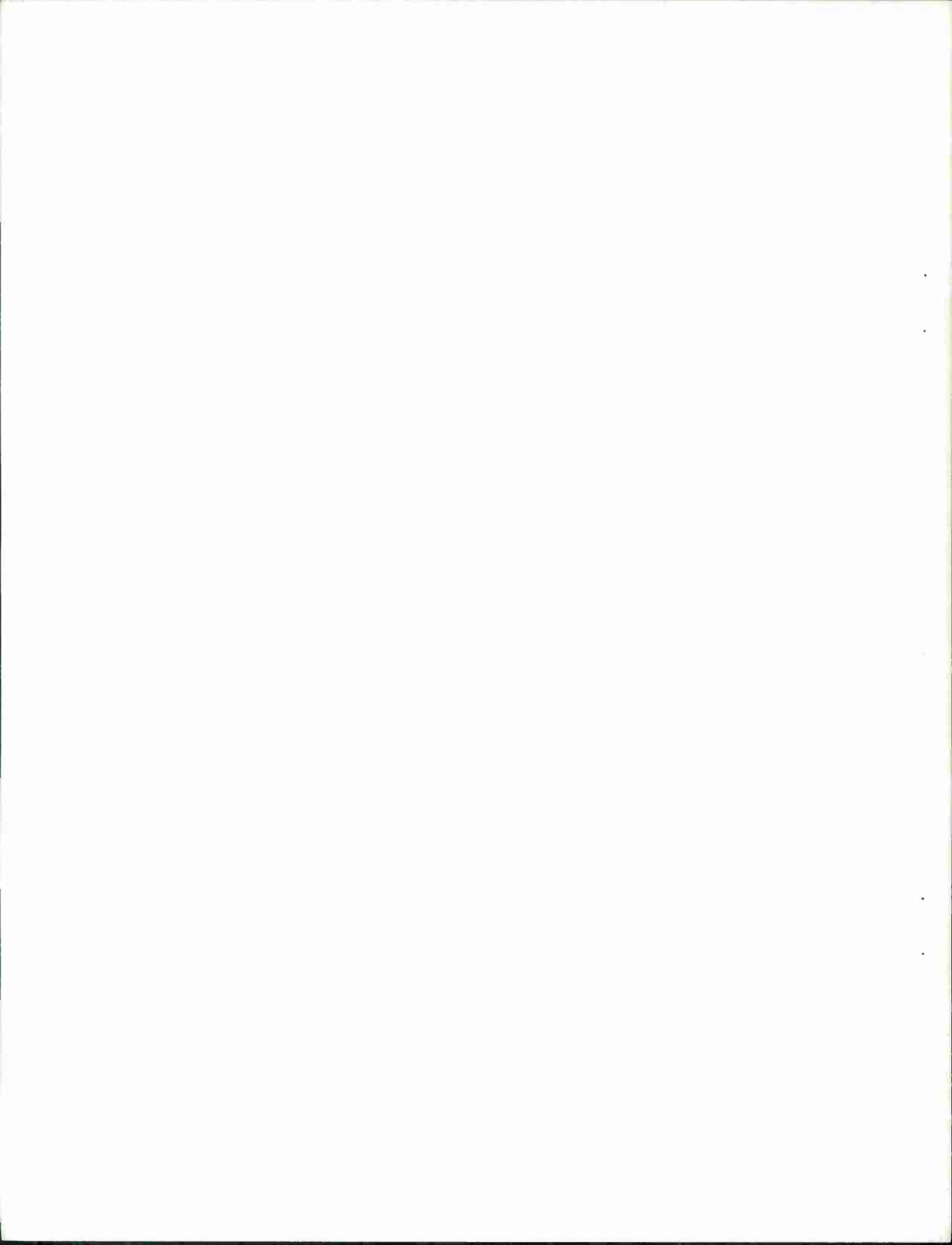
MASSACHUSETTS



## ABSTRACT

The diamond circuit is a gated unity gain amplifier, the principal virtue of which is its extremely high input and output impedance in the Off state. The circuit has a wide variety of uses, but has several drawbacks which limit it at the present time to a few specialized functions. In space electronics, where power is very expensive, the use of diamonds in place of digital elements can provide large savings in power. Diamonds have been flown on several scientific spacecraft including the historic Mariner IV and the recent (16 December 1965) Pioneer VI, both of which are now orbiting the sun.

Accepted for the Air Force  
Franklin C. Hudson,  
Chief, Lincoln Laboratory Office



## I. BASIC CIRCUIT AND OPERATION

The basic diamond circuit is a transistorized version of the versatile four-diode bridge. As a bridge it is self-balancing and inherently temperature stable while it provides large power gain. It has been described<sup>1</sup> as an analog-digital hybrid in the sense that it is an analog logic element having properties which allow it to be used like a digital system building block.

The current and voltage distribution within a perfectly balanced diamond during the application of gate current is shown in Fig. 1. The diamond symbol appears in Fig. 2.

Perfect balance requires that all four transistors have equal gains, base-to-emitter voltages, and emitter currents. A mismatch in any one of these transistor parameters simply alters the current distribution in the balanced circuit, resulting in a small voltage offset between input and output. Additional offset is produced when DC input or output current flows or when the gate currents are not equal. Typically, with unmatched low-power transistors, the offset values are within  $\pm 25$  mv. Matching easily reduces the offsets to  $\pm 1$  mv or less. This suggests using continuous gate current to provide a stable unity-gain isolation amplifier.

For the case of a capacitive load, the output voltage will not generally be equal to the input at the start of a gate current pulse. The bridge will be completely unbalanced by this voltage inequality and only two (diagonally opposite) transistors will be turned on by the gate pulse. During this imbalance the diamond current gain will be its

maximum value  $(\beta+1)^2$ . As the output voltage approaches the input value, the remaining two transistors will be turned on to complete the "self-balancing" of the circuit.

Since balance is achieved only when input and output voltages are equal (discounting offsets), the balanced condition can be used as an indication of voltage equality. Highly accurate voltage comparators operating in a voltage continuum have been built by carefully detecting diamond balance.

An easier implementation of this voltage comparator simply senses the direction of diamond imbalance and acts as a voltage threshold detector. Again, the detection may be anywhere in the voltage continuum offering a significant advantage over the "digital" Schmitt Trigger circuit.

For some applications the basic diamond is purposely modified to provide a fixed voltage offset between input and output. This technique is particularly useful in the production of timing signals and in analog-to-digital (and vice versa) converters.

Offsets may be introduced in a variety of ways, e.g., the insertion of diodes in diagonally opposite legs of the diamond. Resistors, appropriately placed, may be used to produce an offset whose magnitude is determined by the gate current level.

The diamond circuit's versatility in analog systems could be compared with that of the NOR gate in digital systems. Almost any operation can be performed using only diamonds, for example, addition, subtraction, multiplication, logarithms, time delay, and data storage. Unfortunately, the diamond with its associated current drivers is a much more complex building block than the simple NOR gate. This complexity renders

the diamond impractical except in the relatively few cases where it lends itself to simple system realization. The primary example of the latter case is the "sample-and-hold" circuit in which a diamond may replace (functionally) a multi-stage shift register for the temporary storage of data. This diamond function will now be considered in more detail.

## II. STORAGE CAPABILITIES

When diamond gate current is set to zero the input and output impedances become extremely high. The only currents which flow are due to transistor leakages, and the use of high quality, low-leakage silicon devices can provide "Off-resistances" of many hundreds of megohms. This enables a pulsed diamond to "sample" its input voltage at some instant and "hold" that value on an output capacitor for a time interval many orders of magnitude larger than the pulse time required to establish the voltage.

The complexity of a diamond analog memory compared to a digital memory is reduced by the logarithm (base = 2) of as many analog "bits" as can be resolved within the diamond's voltage range. For example, a single diamond having a 12 volt range and 50 mv resolution can store 240 different values (analog "bits"), whereas a digital system requires eight flip-flops to match this requirement. Of course, the diamond cannot store indefinitely, but in many systems only temporary storage is required.

Baker, et al<sup>1</sup>, cite several methods for the rejuvenation of analog signals to provide indefinite storage time in capacitor diamond chains. The most satisfactory approach is that in which a feedback path quantizes the analog levels.

Without rejuvenation the maximum length of hold time,  $T_{\max}$ , depends upon the permissible voltage error because the stored level is continuously degraded by leakage currents into the diamonds and across the storage capacitor itself. Obviously,  $T_{\max}$  may be increased by reducing any or all of the leakage currents.  $T_{\max}$  may also be increased by making the storage capacitor larger providing that the capacitor's leakage does not increase faster than its capacity. Unfortunately, this immediately rules out

all types of electrolytic capacitors, whose leakages tend to be enormous at all values. Many non-electrolytic capacitors have negligible leakage. Thus the major part of the stored voltage "drift" is due to diamond transistor leakages.

Upgraded silicon transistors of the 2N2524 (NPN) and 2N2604 (PNP) variety together with low leakage diodes were assembled to produce extremely low leakage diamonds which were well suited to the sample-and-hold function. Typical offsets of these units were less than 5 mv with  $\pm 1$  mv variation over a temperature range from  $-80$  to  $+150^{\circ}\text{F}$ . Storage times in excess of 15 minutes were obtained with 10 mv accuracy--for a sampling time of  $1\ \mu\text{s}$ . This represents a storage time ratio of about  $10^9$ . The net diamond leakage implied by this experiment is:

$$I_{\text{leak}} = C \frac{dV}{dt} = (1\ \mu\text{F}) \frac{10\ \text{mv}}{1000\ \text{sec}} = 10\ \text{picoamperes}.$$

This current level is comparable to the leakages of the individual semiconductors used except for  $I_{\text{CO}}$  of the 2N2604 which was about 2 na. A special gating technique was used on the 2N2604 to combat this "high" leakage current.

The average power delivered to this diamond over the 15-minute period is, assuming about a 5 volt level,

$$P = \frac{CV^2/2}{T} = \frac{10^{-6} \times 10}{10^3} = 10^{-8} = 10\ \text{nanowatts}.$$

A "state-of-the-art" flip-flop, which stores only a single "bit," is difficult to push down to a power level of 10 microwatts--three orders of magnitude higher.

The above diamond capabilities must be considered in the light of many disadvantages, however. These will be discussed separately.

### III. SEMICONDUCTOR LEAKAGE

Analysis and measurement of transistor leakages in the diamond show that with reference to the input and output terminals these currents tend toward mutual cancellation. In the event of zero leakages or their exact cancellation the input and output resistances are infinite in the Off state. In practice exact cancellation never occurs over any measurable temperature or voltage range and the uncancelled currents flow through the input and output terminals.

Present transistor technology has not produced a PNP device with leakages as small as those of good NPN devices. It is therefore necessary to disconnect the collector of one PNP transistor (during storage) whenever storage times in excess of several seconds are desired. This collector switching, of course, requires additional circuitry which seems to be avoidable only by a more complex diamond system design.

#### IV. TRANSISTOR "β" MINIMUM AND MATCHING

The effect of non-infinite β's is the deterioration of input signal voltages (capacitive input) due to the loading effect of the diamond in its On state. For equal input and output capacitors the minimum transistor β is:

$$\beta_{\min} = \left( \frac{100}{E} \right)^{1/2}, \quad E = \text{allowed \% error in input voltage} .$$

Another significant β consideration exists which is particularly important when the diamond application requires lengthy On state operation with capacitive loading on both input and output. It is shown in Appendix A that continuous-duty operation under these loading conditions is impossible without a near-perfect match of β's for both input and output pairs. Any mismatch tends to cause a deterioration of the input voltage. In fact, some β matching is required even for the normal pulsed operation of the diamond.

Appendix A shows that for a 1% maximum error under typical operating conditions the input transistor pair must not be mismatched by more than 10%. The output pair must not be mismatched by more than 50%. It is also shown that, if the following equation is satisfied, the input errors caused by input and output mismatching will have opposite signs and therefore tend to cancel.

$$\frac{\beta_2 - \beta_4}{\beta_1 - \beta_3} \geq 0 .$$

V. DIELECTRIC ABSORPTION

For storage applications it is desirable to use large value capacitors having low leakage and small volume. Since electrolytic types are ruled out due to high leakages, the best choice for capacity vs. volume and weight would be ceramic capacitors. However, these are strictly ruled out by a phenomenon known as "dielectric absorption." Stress within the dielectric material produces a voltage "rebound" after an initial change of voltage across the capacitor. This effect can be lethal from idle high-voltage capacitor banks whose terminals have not been left in a shorted condition.

The best dielectric for signal storage seems to be polystyrene, but its volume vs. capacity is extremely high. A more practical choice is polycarbonate or metallized mylar. The quality of the latter type is quite dependent on the manufacturing technique, however.

## VI. CONCLUSIONS

The diamond circuit claims a versatility challenged by few other circuits. At the present time, unfortunately, it is practical only in the cases of sample-and-hold functions and variable-voltage threshold detection. This is because of the basic complexity of both the diamond and its current driver--neither of which lend themselves to integrated circuitry (both NPN and PNP transistors are required).

Until the complete diamond and at least part of the driver can be integrated (probably on a multi-chip basis unless the diamond can be built using FET's or other devices) at a reasonable cost it will remain as a specialized circuit for use in low power space electronics.

JDM/lmm

3-63-5383

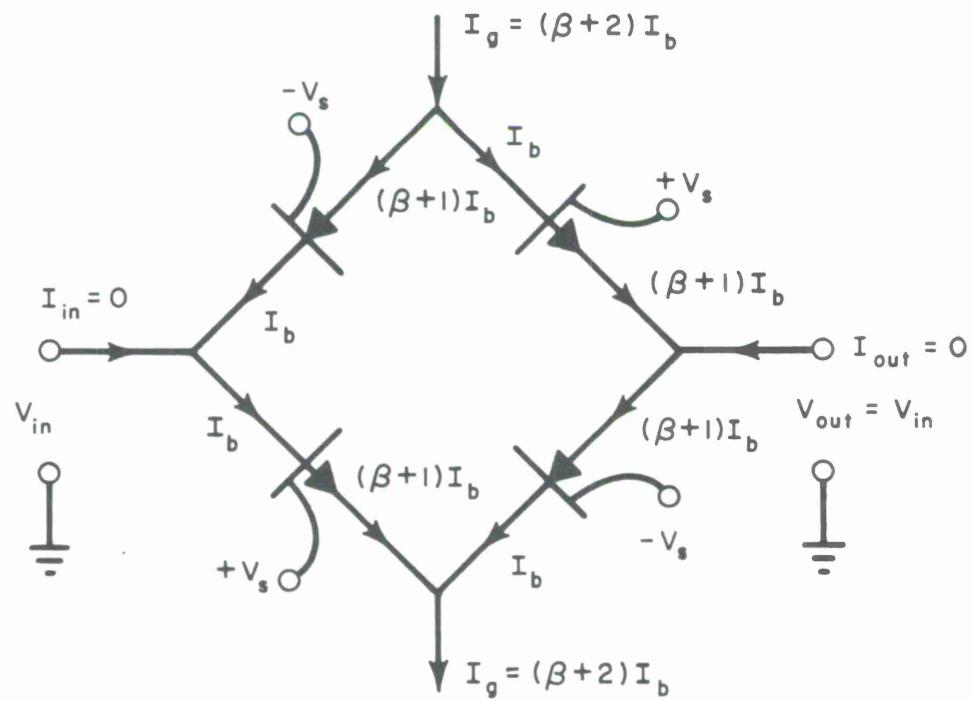


Fig. 1 Current distribution.

3-63-5382

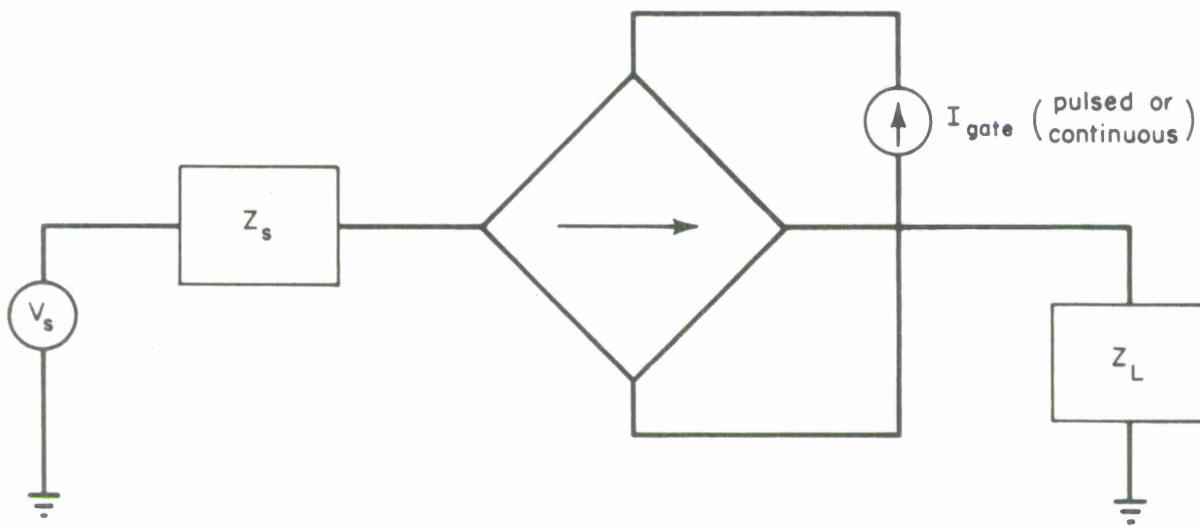


Fig. 2 Diamond symbol.

## REFERENCES

1. R. H. Baker, R. E. McMahon, and R. G. Burgess, "The Diamond Circuit," M. I. T., Lincoln Laboratory Technical Report 300 (30 January 1963).

## APPENDIX A

### TRANSISTOR $\beta$ MATCHING REQUIREMENTS

When the diamond shown below is gated ON, a dynamic transfer of voltage from input to output occurs until the following condition is met:

$$V_{\text{out}} = V_{\text{in}} + V_{\text{offset}} \quad (1)$$

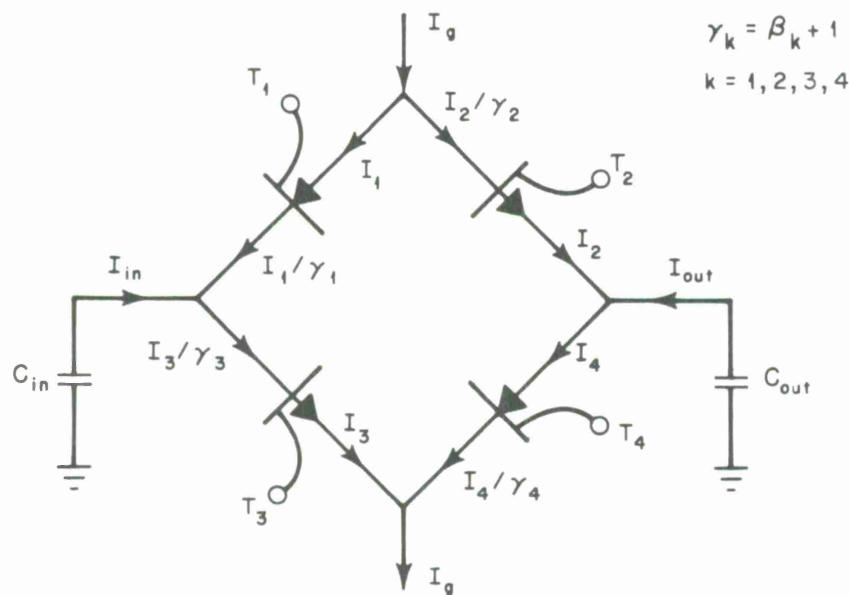
It follows that any further change in voltage conforms to

$$\Delta V_{\text{out}} = \Delta V_{\text{in}}$$

and with  $C_{\text{in}} = C_{\text{out}}$ ,

$$I_{\text{out}} = I_{\text{in}} .$$

3-63-5464



From the figure,

$$I_{\text{out}} = I_4 - I_2 \quad (2)$$

$$I_{\text{in}} = I_3/\gamma_3 - I_1/\gamma_1 \quad (3)$$

$$I_g = I_1 + I_2/\gamma_2 = I_3 + I_4/\gamma_4 . \quad (4)$$

Therefore,

$$I_1 + I_2/\gamma_2 = I_3 + I_2/\gamma_4 + I_{\text{in}}/\gamma_4$$

or

$$I_3 = I_1 + I_2 \left( \frac{1}{\gamma_2} - \frac{1}{\gamma_4} \right) - I_{\text{in}}/\gamma_4 . \quad (5)$$

Substituting this back into Eq. (3) yields

$$I_{\text{in}} = \frac{I_1}{\gamma_3} + I_2 \left( \frac{\gamma_4 - \gamma_2}{\gamma_2 \gamma_3 \gamma_4} \right) - \frac{I_{\text{in}}}{\gamma_3 \gamma_4} - \frac{I_1}{\gamma_1}$$

or

$$I_{\text{in}} \left( 1 + \frac{1}{\gamma_3 \gamma_4} \right) = I_1 \left( \frac{\gamma_1 - \gamma_3}{\gamma_1 \gamma_3} \right) + I_2 \left( \frac{\gamma_4 - \gamma_2}{\gamma_2 \gamma_3 \gamma_4} \right) . \quad (6)$$

The current  $I_n$  will evidently be largest when

$$\begin{aligned} \gamma_3 &= \gamma_1 \left( 1 - \frac{T_{\text{in}}}{100} \right) = \gamma_{\min} \\ \gamma_2 &= \gamma_4 \left( 1 - \frac{T_{\text{out}}}{100} \right) = \gamma_{\min} \end{aligned} \quad (7)$$

where  $T_{in}$  = specified percentage tolerance on input  $\gamma$ 's.

$T_{out}$  = specified percentage tolerance on output  $\gamma$ 's.

$\gamma_{min}$  = specified minimum  $\gamma$ .

Plugging Eq. (7) into Eq. (6) gives

$$I_{in} \left(1 + \frac{1}{\gamma_3 \gamma_4}\right) = I_1 \left(\frac{T_{in}}{100 - T_{in}}\right) \frac{1}{\gamma_1} + I_2 \left(\frac{T_{out}}{100 - T_{out}}\right) \frac{1}{\gamma_3 \gamma_4}. \quad (8)$$

Since all emitter currents ( $I_k$ 's) are roughly equal (normally) to  $I_g$  and  $\gamma_3 \gamma_4 \gg 1$ ,

$$I_{in} < I_g \left[ \left(\frac{T_{in}}{100 - T_{in}}\right) \frac{1}{\gamma_1} + \left(\frac{T_{out}}{100 - T_{out}}\right) \frac{1}{\gamma_3 \gamma_4} \right]. \quad (9)$$

It is clear from Eq. (9) that matching  $\gamma$ 's to about 1 percent will produce  $I_{in}$  currents only about four orders smaller than  $I_g$ . With a drive current  $I_g = 1$  ma and the resulting input current of about 0.1  $\mu$ a, an input capacitor of value 0.1  $\mu$ f suffers a deterioration of

$$\left(\frac{V_{in}}{t}\right) = \frac{I_{in}}{C_{in}} = \frac{0.1 \mu a}{0.1 \mu f} = 1 \text{ volt/sec.}$$

Since larger capacitors are not practical in space vehicle electronics, it is evidently not possible to operate diamonds in continuous-duty applications when the input is capacitively loaded.

Even during pulsed operation this effect is not negligible. If the tolerable error due to input  $\gamma$  mismatch (alone) is arbitrarily set at 10 mv,

$$\Delta V_{in} = \frac{(I_{in}) (\text{pulse time})}{C_{in}} = 10 \text{ mv.}$$

Choosing typical values of  $I_g = 10 \text{ ma}$ ,  $\gamma_{min} = 15$ ,  $C_{in} = 0.1 \mu\text{f}$ , pulse time =  $10 \mu\text{sec}$ ,

$$I_{in} = \frac{(10 \text{ mv}) (0.1 \mu\text{f})}{(10 \mu\text{s})} = 0.1 \text{ ma.}$$

Then, from Eq. (9),

$$[(\frac{T_{in}}{100 - T_{in}}) \frac{1}{15}] 10 \text{ ma} > 0.1 \text{ ma}$$

or

$$T_{in} > 13\% . \quad (10)$$

For the same tolerable error due to output  $\gamma$  mismatch (alone),

$$[(\frac{T_{out}}{100 - T_{out}}) \frac{1}{225}] 10 \text{ ma} > 0.1 \text{ ma}$$

or

$$T_{out} > 69\% . \quad (11)$$

Based on Eqs. (10) and (11), tentative  $\gamma$  matching tolerances may be set at

$$\begin{aligned} T_{in} &= 10\% \\ T_{out} &= 50\% . \end{aligned} \quad (12)$$

Since  $\gamma_{\min}$  will be chosen larger than 10, Eq. (12) may be taken as the  $\beta$  matching requirements.

It may be noted from Eq. (6) that satisfying the following equation will help in minimizing  $I_{in}$ :

$$\frac{\gamma_2 - \gamma_4}{\gamma_1 - \gamma_3} \geq 0$$

or equivalently,

$$\frac{\beta_2 - \beta_4}{\beta_1 - \beta_3} \geq 0. \quad (13)$$

## DISTRIBUTION

### Group 63

Ash, M.	E. Landsman
Ashley, G	Moriarty, B.
Berg, R.	Nathanson, D.
Binsack, J.	Parker, D.
Black, W. L.	Ryan, J.
Bold, D.	Sarles, F. W.
Bowles, L.	Schmidt, W. G.
Braga-Illa, A.	Sferrino, V.
Burrowes, C.	Shapiro, I.
Chick, R.	Sherman, H.
Childs, N.	Sicotte, R.
Connolly, J.	Smith, C.
Crocker, M. C.	Smith, W. B.
Floyd, F. W.	Snider, D.
Grayzel, A.	Stanley, A.
Hoffman, L.	Tang, D.
Howland, B.	Tausner, M.
Mack, C.	Travis, L. J.
MacLellan, D.	Trudeau, N.
Max, J.	Vrablik, E.
McCarron, J.	Waldron, P.
McMahon, R.	Ward, W. W.
Michelove, L.	Weigand, R.
	Whitney, A.

### Division 6

G. P. Dinneen  
W. E. Morrow, Jr.

Group 63 Files (10)

UNCLASSIFIED

Security Classification

**DOCUMENT CONTROL DATA - R&D**

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)



